Contents

1. General Description

The F113/F115/F117 is a high performance, easy to use, single chip ASK Transmitter IC for remote wireless applications in the 300 to 450MHz frequency band. This transmitter IC is a true "data-in, antenna-out" monolithic device. F113/F115/F117 has three strong attributes: power delivery, operating voltage and operating temperature. In terms of power, the F113/F115/F117 is capable of delivering +13dBm into a 50Ω load. This power level enables a small form factor transmitter (lossy antenna) such as a key fob transmitter to operate near the maximum limit of transmission regulations. In terms of operating voltage, the F113/F115/F117 operates from 2.0V to 3.6V. The F113/F115/F117 will work with most batteries to the end of their useful limits. In terms of operating temperature, the F113/F115/F117 operates from -40℃ to +85℃.

The F113/F115/F117 is easy to use. It requires a reference frequency (RF carrier frequency divided by 32 times) generated from a crystal with a few additional external parts to create a complete versatile transmitter.

The F113/F115/F117 operates with ASK/OOK (Amplitude Shift Keying/On-Off Keyed) UHF receiver types from wide-band super-regenerative radios to narrow-band, high performance super-heterodyne receivers. The F113/F115/F117's maximum ASK data rate is 10kbps (Manchester Encoding).

The F113/F115/F117 transmitter solution is ideal for industrial and consumer applications where simplicity and form factor are important.

For enhanced power saving, the F113/F115/F117 includes power managing function. The power managing function Enables transmitter activated as long as high transient data input trigger signals are received. The transmitter will also be automatically switched off if there are no data input transients for a time exceeding approximately 40ms@433.92MHz.

2. Features

- Complete UHF transmitter
- Frequency range 300MHz to 450MHz
- Data rates up to 10kbps ASK
- Output Power to +13dBm
- Low external part count
- Low voltage operation
- Operate with crystals or ceramic resonators
- Power down modes and wake-up functions to reduce power consumption

3. Applications

- Fan Controllers
- Remote Power Switches
- Multi-Media Remote Control
- Remote Sensor Data Links
- Infrared Transmitter Replacement

4. Typical Application

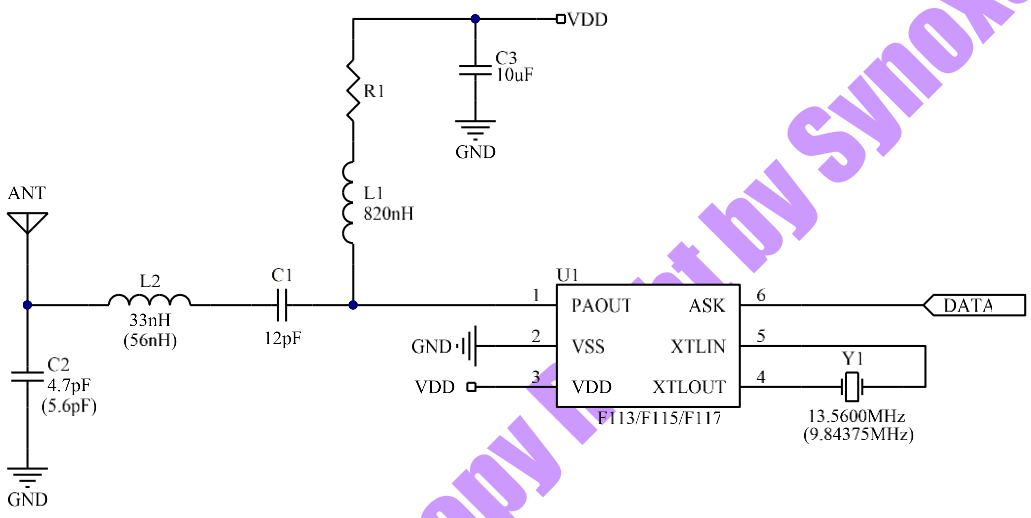
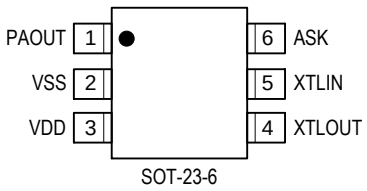


Figure 1. F113/F115/F117 ASK Key Fob Design for 315 MHz and 433.92 MHz
(Note: Values indicated in parentheses are for 315MHz)

5. Pin Configuration



6. Pin Description

Pin Number SOT23-6	Pin Name	Pin Function
1	PAOUT	Power Amplifier Output.
2	VSS	Ground
3	VDD	Voltage Drain Drain (Input): Positive Power Supply

4	XTLOUT	Crystal Out (Output): Reference oscillator output connection
5	XTLIN	Crystal In (Input): Reference oscillator input connection
6	ASK	ASK Data Input

7. Absolute Maximum Ratings (1)

Supply Voltage (V_{DD})	+5V
Input/Output Voltage ($V_{I/O}$)	V_{SS}–0.3 to V_{DD}+0.3
Voltage on PA_OUT(V_{PA_OUT})	+7.2V
Storage Temperature Range (T_S)	–65 ℃ to +150 ℃
Lead Temperature (soldering, 10 sec.)	+300 ℃
ESD Rating	2KV (3)

8. Operating Ratings (2)

RF Frequency Range	300MHz to 450MHz
Supply Voltage (VDD)	+2.0V to +3.6V
Ambient Temperature (T_A)	–40 ℃ to +85 ℃

9. Electrical Characteristics (4)

Specifications apply for VDD = 3.0V, TA = 25 ℃, $Freq_{REFOSC}$ = 13.560MHz. Bold values indicate –40 ℃ to 85 ℃ unless otherwise noted, 1kbps data rate 50% duty cycle. RL 50ohm load (matched)

Parameter	Condition	Min	Typ	Max	Units
Power Supply					
F113/F115/F117 Mark Supply Current I_{ON}	@ 315MHz, POUT = +13dBm		20		mA
	@ 433.92MHz, POUT = +13dBm		20		mA
Standby Mode					
Standby supply current, I_{STB}	@ 315MHz			1	uA
	@ 433.92 MHz			1	uA
Standby delay time	ASK transition from HIGH to LOW		45		ms
	ASK transition from LOW to HIGH		250		us
RF Output Section and Modulation Limits:					
F113/F115/F117 Output power level, P_{OUT} ASK "mark"	@315MHz (4)		+13		dBm
	@433.92MHz (4)		+13		dBm

F113/F115/F117 Harmonics output for 315MHz	@ 630MHz [4] 2nd harm.		-25		dBc
	@945MHz [4] 3rd harm.		-45		dBc
F113/F115/F117 Harmonics output for 433.92 MHz	@ 867.84MHz [4] 2nd harm.		-27		dBc
	@1301.76MHz [4] 3rd harm.		-51		dBc
Extinction ratio for ASK			70		dBc
ASK Modulation					
Data Rate				10	kbps
Occupied Bandwidth	@315MHz [6]		<700		kHz
	@433.92MHz [6]		<1000		kHz
VCO Section					
315 MHz Single Side Band Phase Noise	@ 100kHz from Carrier		-76		dBc/Hz
	@ 1000kHz from Carrier		-79		dBc/Hz
433.92 MHz Single Side Band Phase Noise	@ 100kHz from Carrier		-72		dBc/Hz
	@ 1000kHz from Carrier		-81		dBc/Hz
Reference Oscillator Section					
XTLIN, XTLOUT	Pin capacitance		2		pF
External Capacitance	Not recommended for use		0		pF
Oscillator Startup Time [5]	Crystal: HC49S		300		µs
Digital / Control Section					
Output Blanking	VDD transition from LOW to HIGH		500		µs
Digital Input ASK Pin	High (V_{IH})	$0.8\times V_{DD}$			
	Low (V_{IL})			$0.2\times V_{DD}$	V
Digital Input Leakage Current ASK Pin	High (V_{IH})		0.05		
	Low (V_{IL})		0.05		µA
Under Voltage Lock Out (UVLO)			1.6		V

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
4. Measured using Test Circuit in Figure
5. Dependent on crystal
6. RBW = 100kHz, OBW measured at -20dBc.

10. Test Circuit

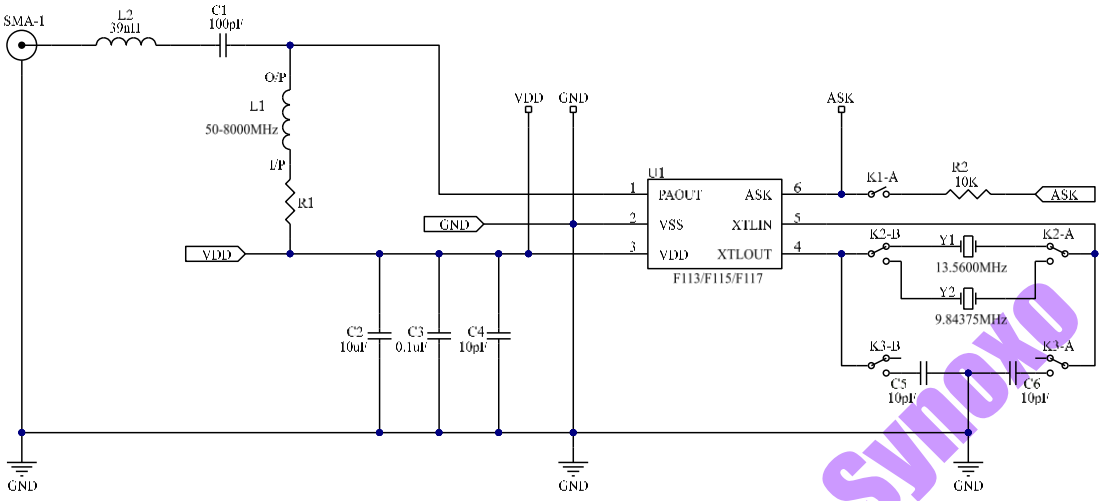
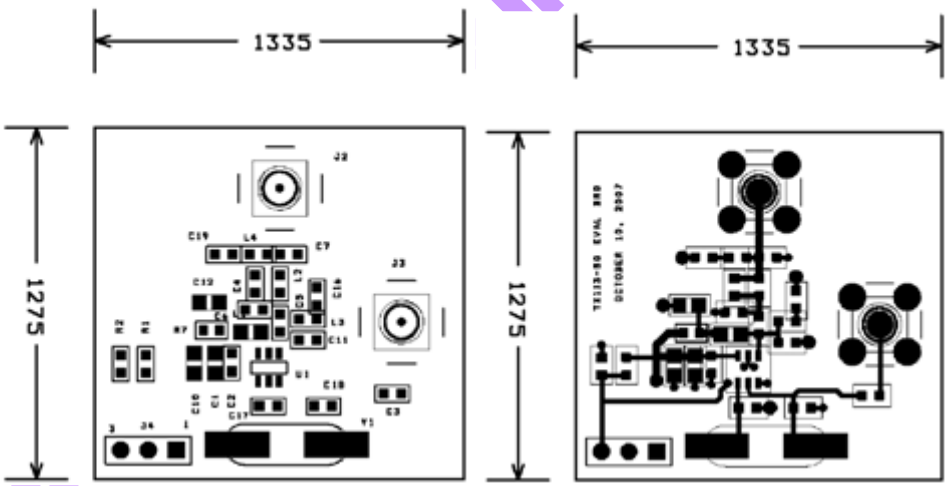


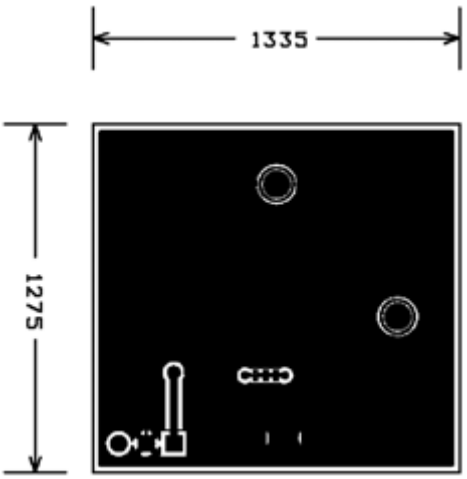
Figure 2. F113/F115/F117 Test Circuit

11. F113/F115/F117 PCB Layout Recommendations



Assembly Drawing
F113/F115/F117 50Ohm Test Board

Top Layer
F113/F115/F117 50Ohm Test Board



Bottom Layer

F113/F115/F117 50Ohm Test Board

12. Functional Diagram

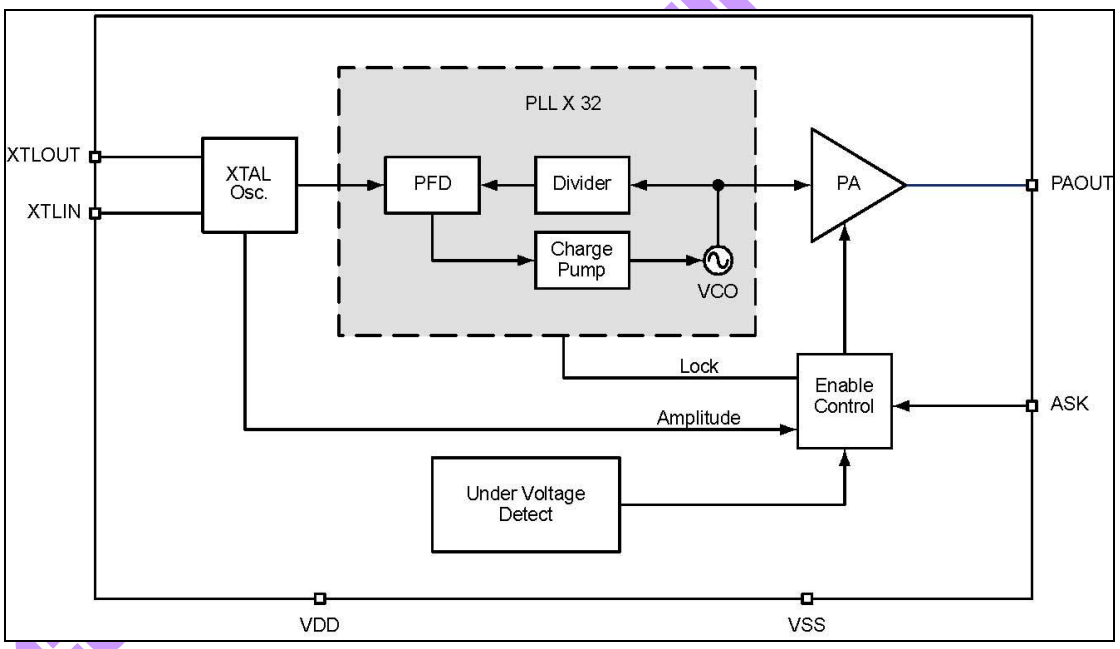


Figure 3. Functional Block Diagram F113/F115/F117

13. Functional Description

Figure 3 is a functional block diagram of the F113/F115/F117 transmitter. The F113/F115/F117 is best described as a phase locked transmitter. The F113/F115/F117 system is partitioned into five functional blocks:

- Crystal oscillator
- PLL ×32
- Power amplifier
- Enable control
- Under voltage detection

13.1. Crystal Oscillator

The reference oscillator is crystal-based Pierce configuration, designed to accept crystals with frequency from 9.375MHz to 14.0625MHz.

13.1.1. Crystal Oscillator Parameters for ASK Operation

Figure 4 shows a reference oscillator circuit configuration for ASK operation. The reference oscillator is capable of driving crystals with ESR range from 20Ω to 300Ω.

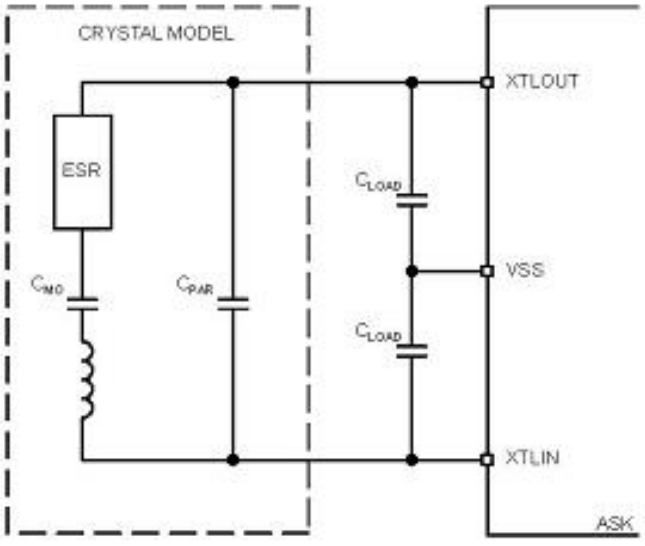


Figure 4. Reference Oscillator ASK Operation

- When the ESR of crystal is at 20Ω, the crystal parameter limits are:
  - ESR 20Ω

- C_{PAR} 2 to 10pF
- C_{MO} 10 to 40fF

- When the ESR of crystal is at 300Ω, the crystal parameter limits are:
  - ESR 300Ω
  - C_{PAR} 2 to 5pF
  - C_{MO} 10 to 40fF
  - C_{LOAD}, not recommended for use.

13.2. PLL ×32

The function of PLL×32 is to provide a stable carrier frequency for transmission. It is a "divide by 32" phase locked loop oscillator.

13.3. Power Amplifier

The power amplifier serves two purposes:

- To buffer the VCO from external elements
- To amplify the phase locked signal. The power amplifier can produce +13dBm at 3V (typical).

13.4. Enable Control

Enable control gates the ASK data. It only allows transmission when Lock, Amplitude and Under Voltage Detect conditions are valid.

13.5. Under Voltage Detect

"Under voltage detect" block senses operating voltage. If the operating voltage falls below 1.6V, "under voltage detect" block will send a signal to "enable control" block to disable the PA.

14. Application Information

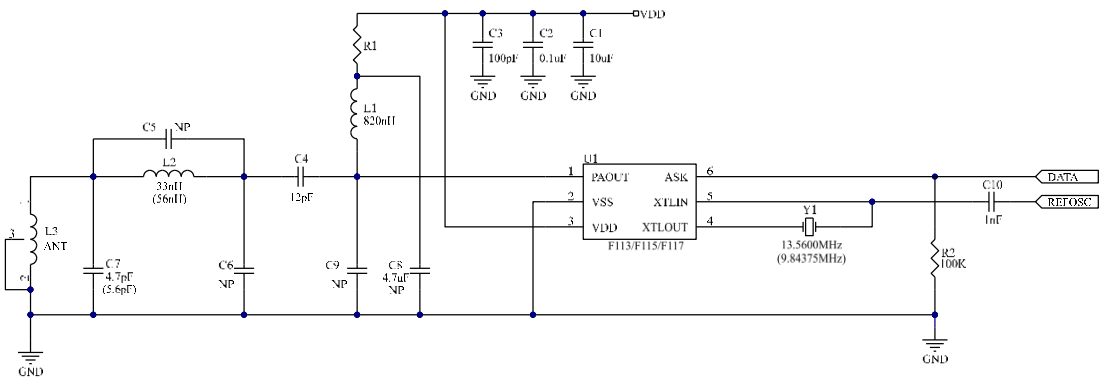


Figure 5. ASK 433.92MHz and (315MHz)

Notes:

1. Components labeled NP are not placed.
2. Values without parentheses are for 433.92 MHz and values in parentheses are for 315MHz.
3. Value of R1 is selected to vary the output power.

The F113/F115/F117 is well suited to drive a 50-ohm source, monopole or a loop antenna. Figure 5 is an example of a loop antenna configuration. Figure 5 also shows both 315MHz and 433.92MHz ASK configurations for a loop antenna. Besides using a different crystal, Table 1 lists modified values needed for the listed frequencies.

Frequency (MHz)	L1 (nH)	C4(pF)	L2 (nH)	C7 (pF)	Y1 (MHz)
315.0	820	12	56	5.6	9.84375
433.92	820	12	33	4.7	13.5600

Table 1

The reference design shown in Figure 5 has an antenna optimized for using the matching network as described in Table 1.

14.1. Power Amplitude Control Using External Resistor

R1 is used to adjust the RF amplitude output levels which may be needed to meet compliance regulation. As shown in Figure 2. R1 of the F113/F115/F117 Demo board using the loop antenna can be adjusted for the appropriate radiated field allowed by FCC or ETSI compliance. Contact Synoxo for suggested R1 values to meet FCC and ETSI compliances.

14.2. Output Power ON-OFF Control

There are three ways to enable the PA output power. First, by supplying the ASK signal with VDD applied continuously, resulting in a Mark and Space RF output condition. Second method involves applying both VDD and ASK synchronously. The third way is using Power Manager Function.

The second method allows for longer battery usage since the battery is disconnected during non-activation. Figure 6 shows the RF output time response since VDD and the ASK are applied to the F113/F115/F117. The RF output response, as a function of VDD, is typically less than 1.25mSec. This measurement was done using the circuitry shown in Figure 2.

Note: The ASK signal should never be applied before VDD.

14.3. RF Output Response as a Function of VDD and ASK

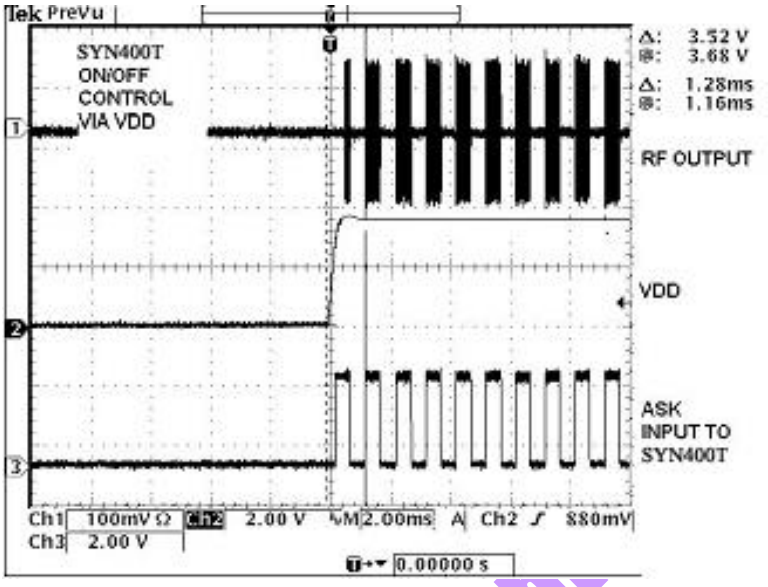


Figure 6. RF Output Response (VDD and ASK)

14.4. Output Matching Network

Part of the function of the output network is to attenuate the second and third harmonics. When matching to a transmit frequency, care must be taken both to optimize for maximum output power, and to attenuate unwanted harmonics.

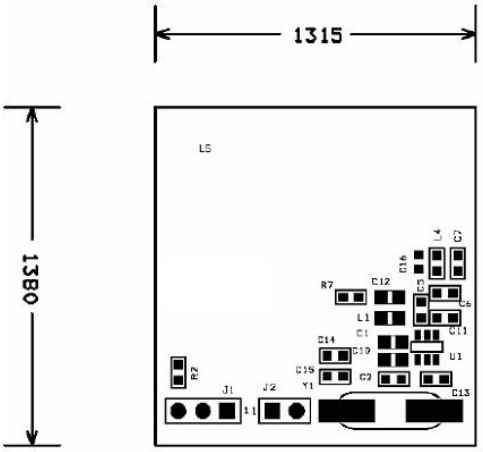
14.5. Layout Issues

PCB Layout is a primary concern for achieving optimum performance and consistent manufacturing results. Care must used with the orientation of components to ensure that they do not couple or decouple the RF signal. PCB trace length should be short to minimize parasitic inductance (1 inch ~ 20nH). For example, depending upon inductance values, a 0.5 inch trace can change the inductance by as much as 10%. To reduce parasitic inductance, the practice of using wide traces and a ground plane under the signal traces is recommended. Vias with low value inductance should be used for components requiring a connection-to-ground.

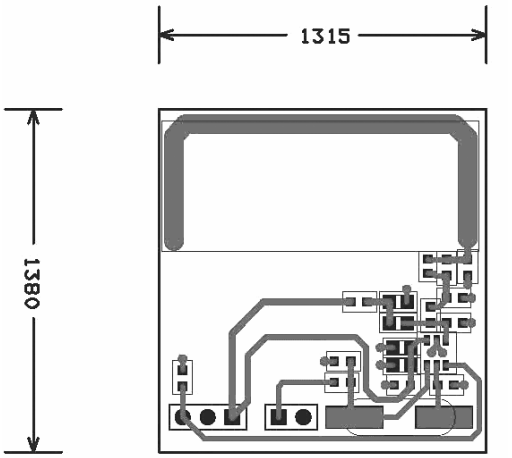
14.6. Antenna Layout

Directivity is affected by antenna trace layout. No ground plane should be under the antenna trace. For consistent performance, components should not be placed inside the loop of the antenna.

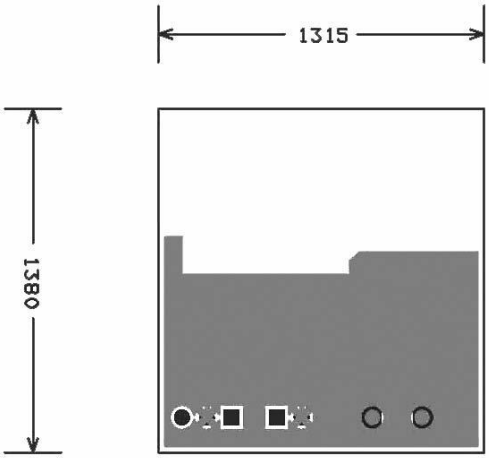
15. PCB Board



Assembly Drawing
F113/F115/F117 Demo Board



Top Layer
F113/F115/F117 Demo Board



Bottom Layer
F113/F115/F117 Demo Board

Figure 7. Demo Board PCB

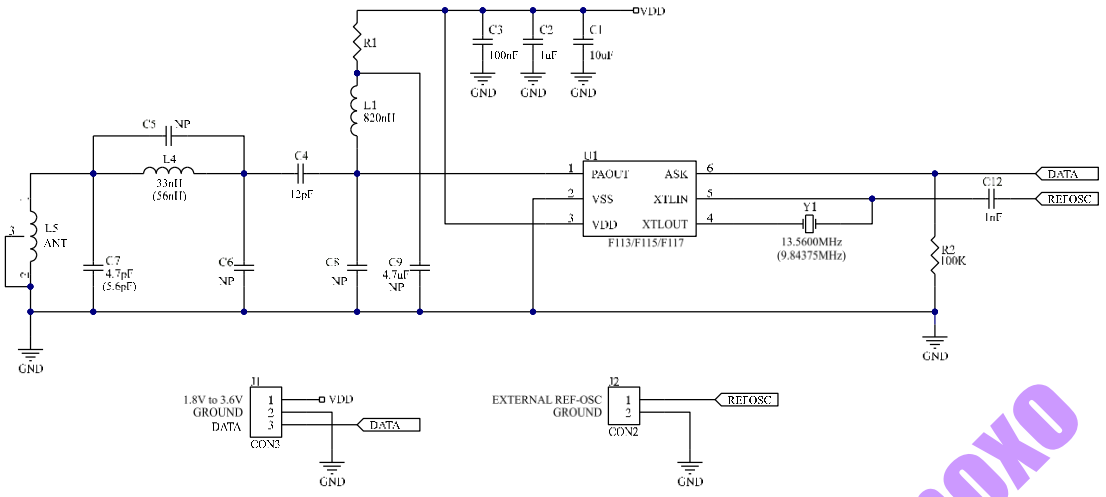
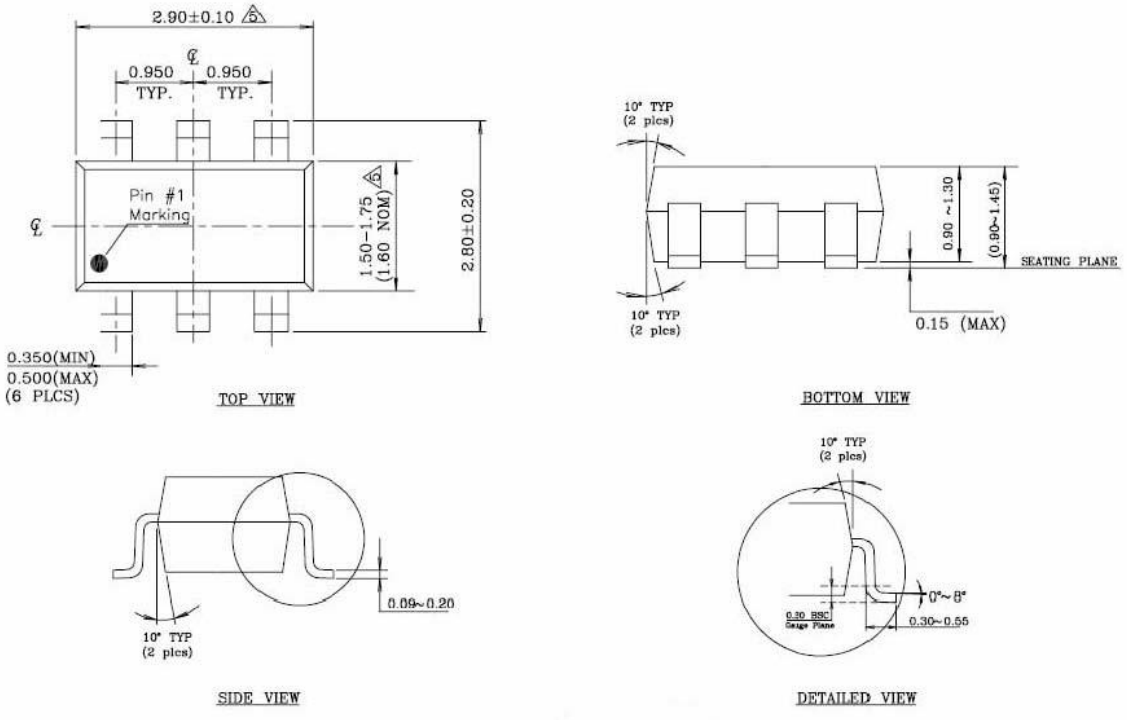


Figure 8. F113/F115/F117 Demo Board Schematic

Notes:

1. Components labeled NP are not placed.
2. Values without parentheses are for 433.92 MHz and values in parentheses are for 315MHz.
3. Value of R1 is selected to vary the output power.

16. Package Information



SOT23-6 Package

附录：注意事项

SYNOXO 新版发射全系列产品（F113/F115/F117/F119）在旧版基础上主要有以下几点的性能提升和应用提示：

1. 相位噪声进一步降低，输出功率统一为+13dBm 典型值。用户可根据实际应用需求，通过选配合适的衰减电阻 R1 进行功率调节和功耗降低。
2. 晶振电路无需外接并联电容，以降低应用成本。
3. 进入休眠模式等待时间缩短为典型值 40ms@433.92MHz 和 50ms@315MHz，以降低应用功耗。

新版发射芯片封装完全兼容旧版，但建议客户外接晶振不再使用负载电容，以免造成客户使用较大负载电容或较大内阻的晶振器件时工作不稳定现象。